A multi Technologies Component Thermal Aspects

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Abstract

A new component is designed by an Israeli start-up, XLoom Photonics Ltd. It is targeted for very high bandwidth interconnections where there is a need to transfer a lot of data to very short distances at very low cost. XLoom's BlueFlame™ Transceiver is targeted at data center rack-to-rack applications such as: Infiniband, Fibre Channel and 10 Gb Ethernet, as well as high-performance computing, shelf extensions and high-speed backplanes.

The product is a multi-channel receiver/transceiver module design, based on a novel technology that uses standard wafer-based processes in order to integrate the VCSEL and Photo-Diodes arrays with the Laser driver, TIA/LA, and optical coupling to fibers, resulting in a very low cost receiver/transceiver capable of transferring up to 40 Gbps to distances up to 300 m.

The BGA type component uses several technologies, such as wire bonding, flip chip, under-fill and encapsulating material. The module is very compact and dissipates 1.4 W for the transmitter and 1.1 W for the receiver unit. The thermal density is moderate but since some of the component internal elements are subjected to derating due to temperature, thermal design was an important part of the design process.

The article will detail the basic elements of the hybrid component design and the thermal design process, the final mechanical and thermal design decisions will be shown.

Key words: thermal analysis, component, silicon substrate, wire bonding

Introduction

A new component targeted for very high bandwidth interconnections, very short distances at very low cost is designed by an Israeli start-up, XLoom Photonics Ltd. The product exhibits a relatively high power generation within a small physical case. CAS designed, analyzed, and solved the component thermal aspects. .

The product is a multi-channel receiver/transceiver module design, based on a novel technology that uses standard wafer based processes in order to integrate the VCSEL and Photo-Diodes arrays with the Laser driver, TIA/LA, and optical coupling to fibers, resulting in a very compact receiver/transceiver capable of transferring up to 40Gbps to distances up to 300m.

The BGA type component assembles the use of different technologies; including wire bonding, flip chip, under-fill and encapsulation processes.

The module dissipates 1.4W for the transmitter and 1.1W for the receiver unit and the thermal density is moderate, however since one of the internal elements is subjected to temperature derating, thermal design is an important part of the development process.

The main issues that this paper deals with are the thermal aspects of this new component design.

Form the thermal point of view the component structure is similar to a BGA. A substrate carries on its upper side the optical part including a coupling port to fibers optics (see figure 1), while the bottom side has solder balls and the most of the transceiver's heated parts, the VCSEL and a Photo-Diodes arrays.

As a result the topside has no power dissipation at all, while all the power generated should be dissipated from the bottom side and thought the solder balls.
The thermal design and simulation intent was to define the best way to handle and take out the generated heat, while keeping the component functionality. Initially, the substrate was planned to be glass, the process described will shows how the first selection was found to be unsuitable to implement. Alternative solutions were proposed and finally implemented as will be shown.

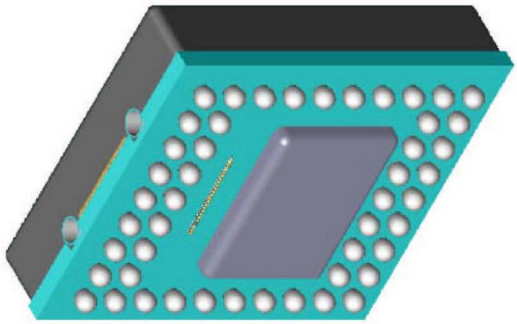

Figure 1: The component general view from the bottom side

Environmental l conditions
In order to determine realistic environmental condition the JEDEC standard (JESD51-6 – Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection) was chosen as the basic boundary condition with some modification:

- Enclosure size: based on JEDEC.
- Board size 114 x 76 mm .
- No additional heat.
- Air speed 1 m/s – in the JEDEC range, a typical and common air speed in Telecom/Datacom chassis system.
- Ta = 55 ^{o}C , based on NEBS GR63 standard, although the JEDEC ambient temperature it determine to Ta= 25-30 ^{o}C.

Thermal model
The Thermal model was solved with **Coolit,** a CFD (Computational Fluid Dynamics) dedicated software for electronic packaging design. CFD models fluid flow and heat transfer on a control volume. The software solves and visualizes the thermal phenomena: conduction, convection and radiation. CFD solves all together the Momentum, Continuity and Energy equations of each cell at the model enclosure.

The model enclosure was based on the JEDEC standard dimensions (see figure 2). An air stream with a velocity of 1 m/s is flows from the edge (see the fan at figure 2) to the other edge, the four other edges of the enclosure are do not allow the air flow, and their net heat flow Q is zero Watt.
As some component parts are extremely small in comparison to the enclosure size, a sub-modeling of the component region was required. The sub-modeling technique enables to solve the very fine details of the model on the sub model scale, extracted from the main model. It enables to keep reasonable element aspect ratio, and solves moderate size models. The model implements a simple and not detailed component in the enclosure and analyses the thermal results on the component scale in the sub-modeling region based on the boundary condition taken from the main model (see figure 3).

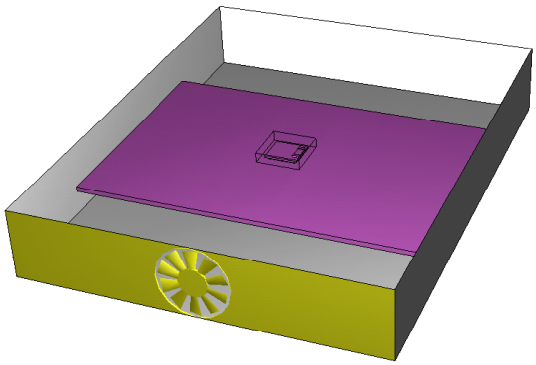

Figure 2: The JEDEC defined enclosure including the component sub model volume

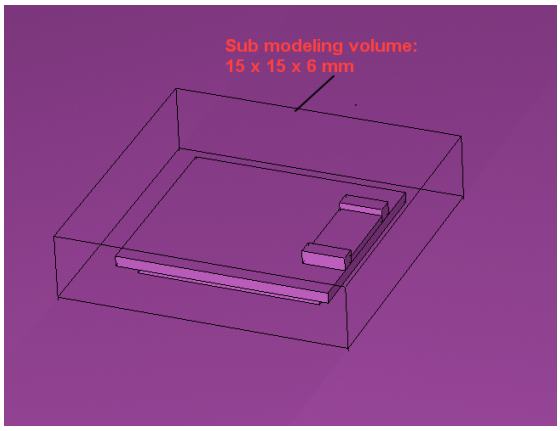

Figure 3: The component sub-modeling region at the main enclosure

The equivalent board conductivity was calculated based on the: JEDEC Standard:

Table 1: PCB conductivity

Layers:		
1 Vcc	1 oz	
1 Ground	1 oz	
4 signal	0.5 oz	
2 pads	1 oz	
Board conductivity		
Kx=Kz=	20	W/m K
Ky=	0.36	W/m K

The component model in the sub model enclosure is seen in figures 4 to 7. The model focuses at bottom side of the component substrate. The integrated circuits Drivers and TIAs are connected by wire bonding to the conductive lines layer (see table 2), and attached to the substrate with a thermal adhesive. The VCSEL and Photo-Diodes array are flip chip connected to the same conductive lines layer, using solder balls that provide electrical and thermal conduction.

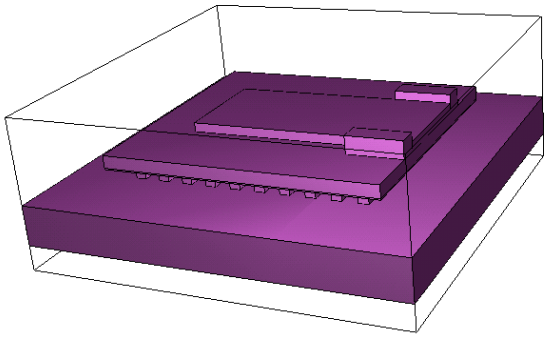

Figure 4: The component sub-modeling region Includes part of the PCB and the details component

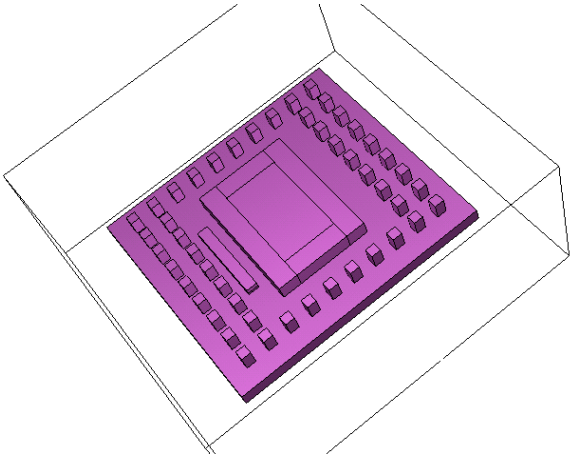

Figure 5: The component model from bottom side including the solder balls, driver, VCSEL, the Photo-Diodes arrays with the encapsulation material (the PCB is hidden).

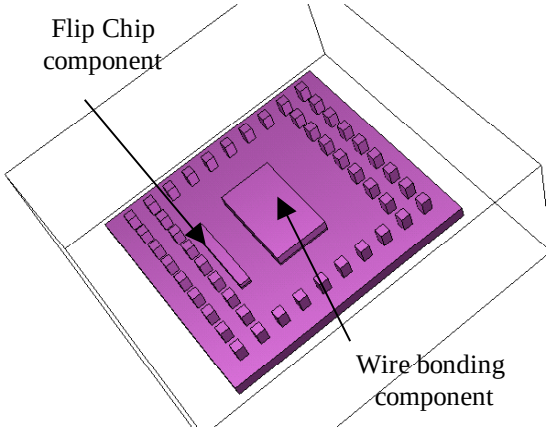

Figure 6: The component model from bottom side including the solder balls, driver, VCSEL, the Photo-Diodes arrays, without the encapsulation material (the PCB is hidden).

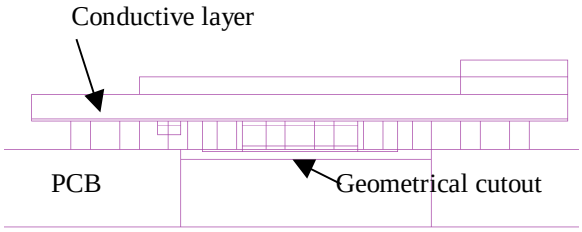

Figure 7: The component model cross section at a wire frame view.

The solder balls are contact to a conduction layer of 2.5 µm thickness, as the layer is very thin it was assumed to be 0.05 mm in the model and the conductivity was corrected in all 3 axis.

Table 2: conduction layer conductivity

Conduction layer		
Aluminum	0.7 µm	
Alumina	0.2 µm	
Nickel	1.5 µm	
Gold	0.1 µm	
Total	2.5 µm	
Corrected Conductivity		
Kx=kz=	1.8	W/m K
Ky=	720	W/m K

Assumption:

- H2OE glue at the VCSEL base 0.1 mm thickness.
- The wire bonding conductivity was neglected.
- Flip chip equivalent solder balls thermal resistance at the Photo-Diodes arrays K= 15 W/m K

- Equivalent thermal conductivity due to the via's, is the same as table 1 for lateral PCB direction and assume to be 7 W/m K at the perpendicular to the PCB direction.
- No resistance between the solder balls and the PCB top layer.
- The solder balls cross section were assumed based on the common connection area.

Table 3: Material properties

Function	***Material***	***Conductivity***
		W/m K
substrate base	Glass	1
	Silicon	150
glue	H2OE	29
solder balls	Lead 90/10	50
Encapsulate cover	EP729	0.42

Table 4: Powers

Components	***Nominal Power***
	mW
VCSEL Driver Pd	1330
VCSEL Array Pd	72
Total	**1402**

Throughout the design process different possibilities where evaluated. Out of the basic idea of a glass substrate, based on the high temperature requirements some modification where proposed and simulated:

1. **Case 1** - Basic case with glass substrate.
2. **Case 2** - Basic case with silicon substrate instead of glass.
3. **case 3** - Basic case with thermal pad connecting the encapsulation material to the PCB.
4. **case 4** - Same as case 2 with add via's to the PCB to increase the board conductivity.

Results

The following paragraph summarizes the thermal simulation results. Table 5 shows a summary of the case temperature at the VCSEL driver and at the Photo-Diodes arrays.
The figure shows the temperature distribution and the heat flux for the different case at the central cross section view. Note that the legend has different heat scales as the maximum temperature of each case is different.

Table 5: Results summary - Driver and Arrays case temperature

Case description	*Power*	*Base*	*Driver case Temp.*	*Array case Temp.*
	[mW]		[C]	[C]
Basic	1402	Glass	214	135
Silicon base	1402	Silicon	90	88
Basic +pad	1402	Glass	127	104
Basic +silicon+via's	1402	Silicon	76	74

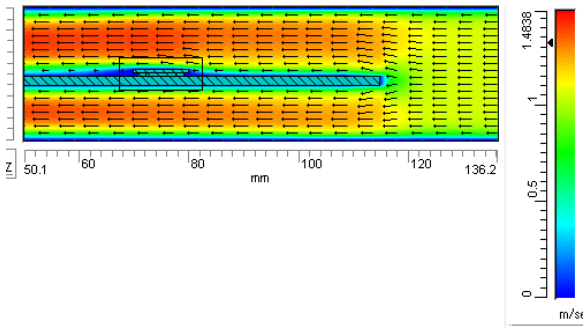

Figure 8: air velocity at the main model
The flow velocity over the sub- model can be seen
It was taken as the B.C for the sub-modeling

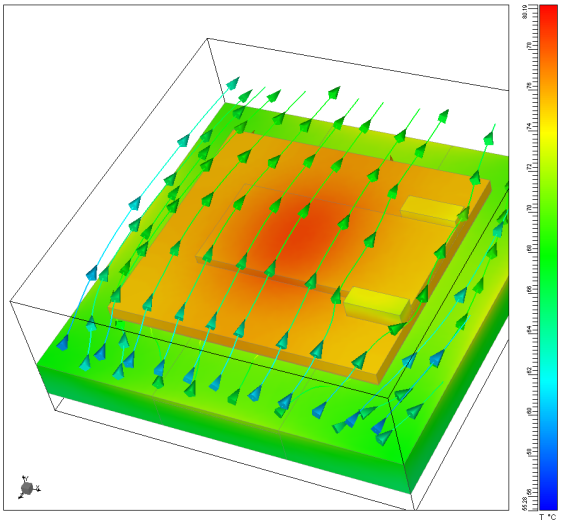

Figure 9: air velocity vector at the sub model from the main model B.C.

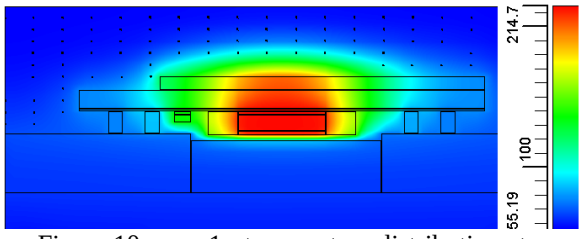

Figure 10: case-1 - temperature distribution at a central cross section

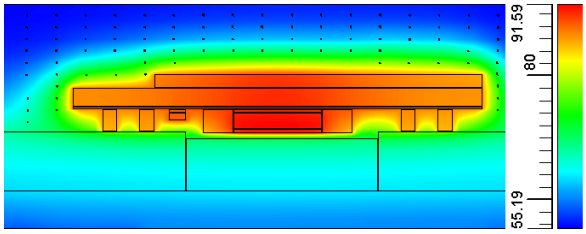

Figure 11: case-2 - temperature distribution at a central cross section

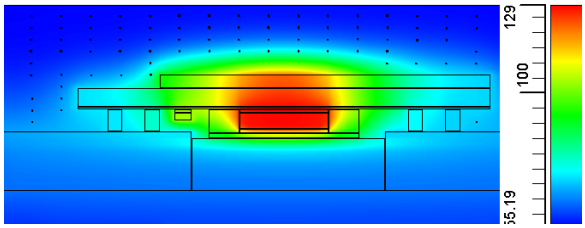

Figure 12: case-3 - temperature distribution at a central cross section

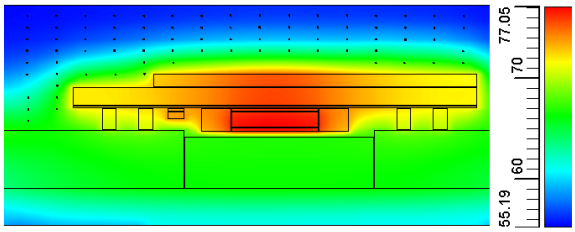

Figure 13: case-4 - temperature distribution at a central cross section

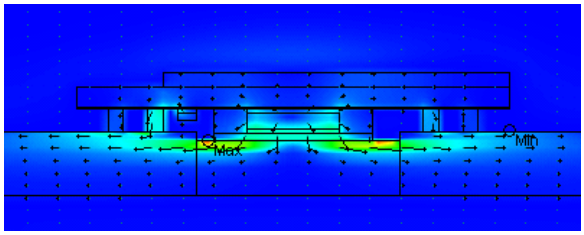

Figure 14: case-3 - Heat flex map from the VCSEL and the Photo-Diodes arrays to the PCB

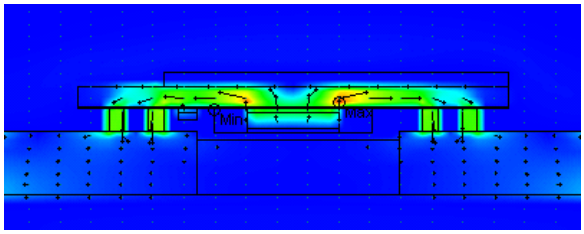

Figure 15: case-4 - Heat flex map from the VCSEL and the Photo-Diodes arrays to the PCB

Summary and conclusion

The above work demonstrates the importance of thermal simulation throughout the design process. The results clearly show the temperature reduction improvement at the VCSEL driver and the Photo-Diodes arrays. The optimized design achieved reasonable temperatures following the suggested improvement, eliminating the need for a Heat Sink.
It was shown that the component substrate must be formed from a more conductive material then glass – silicon was chosen with a conductivity 2 orders of magnitude higher then glass. The direct heat dissipation through pad did not achieve the required results and it is more complicated to implement. The additional via's at the PCB level helped to dissipate the heat from the solder balls to the PCB layers.